IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Park et al. | Docket No.: TI-35623

Serial No.: 10/628,198 | Confirmation No: 6116

Filed: 07/28/2003 | Examiner: Chambliss, A.

Art Unit: 2814

Title: A Two-Step Semiconductor Manufacturing Process for Copper Interconnects

APPEAL BRIEF UNDER 37 CFR§1.192

May 15, 2006

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, Virginia 22313-1450

Dear Sir:

Pursuant to the final Office Action dated 02/21/2006, the Appellants submit this Appellants' Brief. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

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REAL PARTY IN INTEREST

The Real Party in Interest in the present appeal is Texas Instruments Incorporated, the assignee, as evidenced by the assignment set forth at Reel 014687, Frame 0455.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to the Appellants.

STATUS OF CLAIMS

Claims 1-8 are the subject of this appeal. Claims 1-8 are pending; Claims 1, 3, and 5-8 are rejected, and Claims 2 and 4 are objected to

STATUS OF AMENDMENTS

The Appellants did not file any amendment subsequent to the final Office Action dated February 21, 2006.

SUMMARY OF THECLAIMED SUBJECT MATTER

Independent Claim 1 is directed to a method (FIG. 3, page 3 line 9 through page 7 line 3) for manufacturing copper interconnects (element 30, 30a and 30b of FIGS. 1 and 2, page 3 lines 9 -10) on a semiconductor wafer (element 10 of FIGS. 1 -2 and 4-6, page 2 line 24 , page 3 line 1) . The method includes forming a layer of patterned dielectric material (element 300 of FIG. 3, page 3 lines 10 -12) where the patterned dielectric material defines spaces for the copper interconnects (FIG. 4, page 3 lines 12 -14). The method also includes depositing a copper seed layer (element 30c of FIGS. 4-6, element 310 of FIG. 3, page 3 line 20) over the layer of patterned dielectric material. In addition, the method includes depositing a first layer of copper grains (element 30d of FIGS. 5 and 6, element 320 of FIG. 3, page 4 lines 1 -15) having a first initial grain size (page 4 lines 14-15 and 21-25, page 5 lines 1-18) over the copper seed layer, where the first layer of copper grains are deposited by an electroplating process (FIG. 5, page 4 lines 1 -15). Furthermore, the method includes depositing a second layer of copper grains (element 30e of FIG. 6, element 330 of FIG. 3, page 4 lines 17 -25, page 5 lines 1-18) having a second initial grain size (page 4 lines 18 -25, page 5 lines 1 -18) over the first layer of copper grains having the first initial grain size (FIG. 6, page 4 lines 17 -25, page 5 lines 1 -18), the second layer of copper grains being deposited by an electroplating process (page 4 lines 17-25, page 5 lines 1-18).

Claim 2 is dependent on Claim 1 and further specifies the additional step of depositing at least one additional layer of copper grains of any initial grain size over the second layer of copper grains (element 330 of FIG. 3, page 4 lines 21 -25), where the at least one additional layer of copper grains is deposited by an electroplating process (page 4 lines 21-25).

Claim 3 is dependent on Claim 1 and further specifies that the first initial grain size is smaller than the second initial grain size (page 4 lines 11-20).

Claim 4 is dependent on Claim 2 and further specifies that the initial grain size of the at least one additional layer of copper grains is larger than the first initial grain size (page 4 lines 21-25).

Claim 5 is dependent on Claim 1 and further specifies the additional step of annealing the semiconductor wafer (element 340 of FIG. 3, page 5 lines 20 -24, page 6 lines 1-2) after the step of depositing a second layer of copper grains (element 330 of FIG. 3).

Claim 6 is dependent on Claim 5 and further specifies that the annealing step is performed within a temperature range of 100º C to 300º C for a time between 10 minutes to 60 minutes (page 6 lines 1-2).

Independent Claim 7 is directed to a method (FIG. 3, page 3 line 9 through page 7 line 3) for manufacturing copper interconnects (element 30, 30a and 30b of FIGS. 1 and 2, page 3 lines 9 -10) on a semiconductor wafer (element 10 of FIGS. 1 -2 and 4-6, page 2 line 24 and page 3 line 1). The method includes forming a layer of patterned dielectric material (element 300 of FIG. 3, page 3 lines 10 -12) where the patterned dielectric material defines spaces for the copper interconnects (FIG. 4, page 3 lines 12-14). The method also includes depositing a copper seed layer (element 30c of FIGS. 4-6, element 310 of FIG. 3, page 3 line 20) over the layer of patterned dielectric material. In addition, the method includes depositing a first layer of copper grains (element 30d of FIGS. 5 and 6, element 320 of FIG. 3, page 4 lines 1 -15) having a first initial grain size (page 4 lines 14 -15, and 21 -25, page 5 lines 1 -18) over the copper seed layer, where the first layer of copper grains are deposited by an electroplating process (FIG. 5, page 4 lines 1-15). Furthermore, the method includes depositing at least one additional layer of copper grains (element 30e of FIG. 6, element 330 of FIG. 3, page 4 lines 21-25) of differing initial grain sizes (page 4 lines 21-22) over the first layer of copper grains having the first initial grain size (FIG. 6, page 4 lines 17 -25, page 5 lines 1 -18), the at least one additional layer of copper grains being deposited by an electroplating process (page 4 lines 17-25).

Independent Claim 8 is directed to a method (FIG. 3, page 3 line 9 through page 7 line 3) for manufacturing copper interconnects (element 30, 30a and 30b of FIGS. 1 and 2, page 3 lines 9 -10) on a semiconductor wafer (element 10 of FIGS. 1 -2 and 4-6, page 2 line 2 4 and page 3 line 1). The method includes forming a layer of patterned dielectric material (element 300 of FIG. 3, page 3 lines 10 -12) where the patterned dielectric material defines spaces for the copper interconnects (FIG. 4, page 3 lines 12 -14). The method also includes depositing a copper seed layer (element 30c of FIGS. 4-6, element 310 of FIG. 3, page 3 line 20) over the layer of patterned dielectric material. In addition, the method includes depositing a first layer of copper grains (element 30d of FIGS. 5 and 6, element 320 of FIG. 3, page 4 lines 1 -15) having a first initial grain size (page 4 lines 14 -15, and 21 -25, page 5 lines 1 -18) over the copper seed layer, where the first layer of copper grains are deposited by an electroplating process (FIG. 5, page 4 lines 1 -15). Furthermore, the method includes depositing a second layer of copper grains (element 30e of FIG. 6, element 330 of FIG. 3, page 4 lines 17 -25, page 5 lines 1-18) having a second initial grain size (page 4 lines 18 -25, page 5 lines 1-18) over the first layer of copper grains having the first initial grain size (FIG. 6, page 4 lines 17 -25, page 5 lines 1 -18), the second layer of copper grains being deposited by an electroplating process (page 4 lines 17 -25, page 5 lines 1 -18). Moreover, the method includes annealing the semiconductor wafer (element 340 of FIG. 3, page 5 lines 20 -24, page 6 lines 1-2).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1, 3, 7, and 8 stand rejected under 35 U.S.C. §102(e) as being anticipated by the patent granted to Park et al. (U.S. Pat. No. 6,709,970).

2. Claims 5-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the patent granted to Park et al. (U.S. Pat. No. 6,709,970) in view of the patent granted to Uzoh et al. (U.S. Pat. No. 6,861,354).

ARGUMENT

1. Rejection under 35 U.S.C. §102(e) over the patent granted to Park et al. (U.S. Pat. No. 6,709,970)

Claim 1

Independent Claim 1 positively recites depositing a first layer of copper grains having a first in itial grain size over a copper seed layer, the first layer of copper grains being deposited by an electroplating process; and depositing a second layer of copper grains having a second initial grain size over the first layer of copper grains having the first initial grain size , the second layer of copper grains being deposited by an electroplating process . These advantageously claimed features are not taught or suggested by the patent granted to Park et al.

Park et al. teaches away from the advantageously claimed invention by teaching the formation of a second Cu layer 130 over a first Cu layer 110 in which the copper grains of the first copper layer 100 were changed by an annealing process to form a first copper layer 110 (column 2 lines 36-38 and 64-66, column 3 lines 32-34, column 5 lines 49-54, column 6 lines 12 and 33-35, FIGS. 5-6). Park et al. does not teach the formation of a second layer of copper grains (having a second initial grain size) over a first layer of copper

grains that still have the first initial grain size (i.e. the first layer of copper grains 100 that have not been modified by the annealing process to form layer 110), which is advantageously claimed. This is because Park et al. teaches an annealing step that is a "necessary" treatment following the deposition of the first layer of Cu grains to intentionally "increase the grain size" (column 4 lines 32-34 and 45-47, column 5 lines 49-54, see also column 2 lines 34 -35 and 61 -65 and column 3 lines 29 -31). In summary, Park et al. teaches away from the advantageously claimed invention because Park et al. states that an annealing step between the deposition of the first and second layer of copper film is a "necessary" step after the deposition of the first electroplating film and before the deposition of the second copper film in order to "form a stable and generally void -free structure that, after annealing, is compatible with a subsequent thicker (large-grained) Cu layer created in a next cavity -filling deposition process" (column 4 lines 36-39, see also column 5 lines 50-54). Moreover, Park et al. teaches that the grain size of the first layer is increased before the deposition of the second layer of copper (column 5 lines 50 -51) so Park et al. does not teach " depositing a second layer of copper grains … over the first layer of copper grains having the first initial grain size" as advantageously claimed. The Appellants also submit that the claimed process – whereby there is no anneal step between the formation of the first and second l ayer of copper grains – avoids the problem of the unwanted insulating copper oxide film that is noted in Park et al. (column 6 lines 11-18).

Therefore, Claim 1 is patentable over the patent granted to Park et al.

Claim 3

Claim 3 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 3 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patent granted to Park et al. Namely, Claim 3 further specifies the additional limitation that the first initial grain size is smaller than the second initial grain size.

Park et al. does not teach Claim 3 because Park et al. does not teach depositing a second layer of copper grains having a second initial grain size over the first layer of copper grains still having the first initial grain size that is smaller than the second initial grain size, as advantageously claimed. Rather, Park et al. teaches that the grain size of the first layer is increased before the deposition of the second layer of copper (column 5 lines 50-51).

Therefore, Claim 3 is patentable over the patent granted to Park et al.

Claim 7

Independent Claim 7 positively recites depositing at least one additional layer of copper grains of differing initial grain sizes over the first layer of copper grains having the first initial grain size, the at least one additional layer of copper grains being

deposited by an electroplating process. These advantageously claimed features are not taught or suggested by the patent granted to Park et al.

Park et al. teaches away from the advantageously claimed invention because Park et al. states that the second layer of copper grains are a uniform (and larger) grain size (column 4 lines 37-40, column 6 lines 30-32 and 41-47). Therefore, Park et al. does not teach depositing at least one additional layer of copper grains of differing initial grain sizes as advantageously claimed.

Moreover, Park et al. teaches away from the advantageously claimed invention by teaching the formation of a second Cu layer 130 over a first Cu layer 110 in which the copper grains of the first copper layer 100 were changed by an annealing process to form a first copper layer 110 (column 2 lines 36-38 and 64-66, column 3 lines 32-34, column 5 lines 49-54, column 6 lines 12 and 33-35, FIGS. 5-6). Park et al. does not teach the formation of at least one additional layer of copper grains (having differing grain sizes) over a first layer of copper grains that still have the first initial grain size (i.e. the first layer of copper grains 100 that have not been modified by the annealing process to form layer 110), which is advantageously claimed. This is because Park et al. teaches an annealing step that is a "necessary" treatment following the deposition of the first layer of Cu grains to intentionally "increase the grain size" (column 4 lines 32-34 and 45-47, column 5 lines 49-54, see also column 2 lines 34-35 and 61-65 and column 3 lines 29-31). In summary, Park et al. teaches away from the advantageously claimed invention because Park et al. states that the second layer of copper grains are a uniform (and larger) grain size (column 4 lines

37-40, column 6 lines 30-32 and 41-47). In addition, Park et al. teaches away from the advantageously claimed invention because Park et al. states that an annealing step between the deposition of the first and second layer of copper film is a "necessary" step after the deposition of the first electroplating film and before the deposition of the second copper film in order to "form a stable and generally void-free structure that, after annealing, is compatible with a subsequent thicker (large-grained) Cu layer created in a next cavity-filling deposition process" (column 4 lines 36-39, see also column 5 lines 50-54). Moreover, Park et al. teaches that the grain size of the first layer is increased before the deposition of the second layer of copper (column 5 lines 50-51) so Park et al. does not teach "depositing at least one additional layer of copper grains ... over the first layer of copper grains having the first initial grain size" as advantageously claimed. The Appellants also submit that the claimed process whereby there is no anneal step between the formation of the first and second layer of copper grains – avoids the problem of the unwanted insulating copper oxide film that is noted in Park et al. (column 6 lines 1-8).

Therefore, Claim 7 is patentable over the patent granted to Park et al.

Claim 8

Independent Claim 8 positively recites depositing a second layer of copper grains having a second initial grain size over the first layer of copper grains having the first initial grain size. In addition, Claim 8 positively recites the step of annealing the semiconductor wafer after the step of depositing the second layer of copper grains.

These advantageously claimed features are not taught or suggested by the patent granted to Park et al.

The Appellants respectfully traverse the assertion in the Office Action (page 6) that Park et al. teaches - in column 5 lines 49 -50 - the step of annealing the semiconductor wafer after the deposition of the second metal film. The Appellants submit that Park et al. only teaches the use of an anneal step after the deposition of the first metal film (column 2 lines 35-36 and 62-64, column 3 lines 29-33, column 4 lines 36-37, column 5 lines 49-51). Furthermore, the Appellants submit that Park et al. teaches away from the use of an anneal step after the deposition of the second metal film by teaching that the planarization step is performed "immediately" after the second metal film is deposited (column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Moreover, Park et al. teaches away from the advantageously claimed invention by teaching the formation of a second Cu layer 130 over a first Cu layer 110 in which the copper grains of the first copper layer 100 were changed by an annealing process to form a first copper layer 110 (column 2 lines 36-38 and 64-66, column 3 lines 32-34, column 5 lines 49-54, column 6 lines 12 and 33 -35, FIGS. 5 -6). Park et al. does not teach the formation of a second layer of copper grains (having a second initial grain size) over a first layer of copper grains that still have the first initial grain size (i.e. the first layer of copper grains 100 that have not been modified by the annealing process to form layer 110), which is advantageously claimed. This is because Park et al. teaches an annealing step that is a "necessary" treatment following the deposition of the first layer of Cu grains to intentionally

"increase the grain size" (column 4 lines 32-34 and 45-47, column 5 lines 49-54, see also column 2 lines 34 -35 and 61 -65 and column 3 lines 29 -31). In summary, Park et al. teaches away from the advantageously claimed invention because Park et al. states that an annealing step between the deposition of the first and second layer of copper film is a "necessary" step after the deposition of the first electroplating film and before the deposition of the second copper film in order to "form a stable and generally void-free structure that, after annealing, is compatible with a subsequent thicker (large-grained) Cu layer created in a next cavity-filling deposition process" (column 4 lines 36-39, see also column 5 lines 50-54). Moreover, Park et al. teaches that the grain size of the first layer is increased before the deposition of the second layer of copper (column 5 lines 50-51) so Park et al. does not teach "depositing a second layer of copper grains … over the first layer of copper grains having the first initial grain size" as advantageously claimed. The Appellants also submit that the claimed process – whereby there is no anneal step between the formation of the first and second layer of copper grains – avoids the problem of the unwanted insulating copper oxide film that is noted in Park et al. (column 6 lines 1-8).

Therefore, Claim 8 is patentable over the patent granted to Park et al.

2. Rejection under 35 U.S.C. §103(a) over the patent granted to Park et al. (U.S. Pat. No. 6,709,970) in view of the patent granted to Uzoh et al. (U.S. Pat. No. 6,861,354).

Claim 5

Claim 5 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 5 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patents granted to Park et al. or Uzoh et al.; either alone or in combination. Namely, Claim 5 further specifies the additional step of annealing the semiconductor wafer after the step of depositing a second layer of copper grains.

Uzoh et al. does not teach the advantageously claimed invention because Uzoh et al. teaches an anneal step that is used in a completely different process. Specifically, Uzoh et al. teaches away from the advantageously claimed invention by teaching a process where the first conductive layer is modified (by planarization and annealing) before the formation of the second conductive layer (column 4 lines 25-34 and 62-67, column 5 lines 1-35), but not the formation of a second layer of copper grains over a first layer of copper grains having the first initial grain size as is advantageously claimed. As stated in column 1 lines 35-36, annealing promotes grain growth. The planarization process also

modifies the grain size of the first conductive layer (column 5 lines 3-67, column 6 lines 1-28).

The Appellants respectfully traverse the assertion in the Office Action (page 7) that Park et al. teaches - in column 5 lines 49 -50 - the step of annealing the semiconductor wafer after the deposition of the second metal film. The Appellants submit that Park et al. only teaches the use of an anneal step after the deposition of the first metal film (column 2 lines 35-36 and 62-64, column 3 lines 29-33, column 4 lines 36-37, column 5 lines 49-51). Furthermore, the Appellants submit that Park et al. teaches away from the use of an anneal step after the deposition of the second metal film by teaching that the planarization step is performed "immediately" after the second metal film is deposited (column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Furthermore, the Appellants submit that one skilled in the art would not combine the teachings of an interconnect fabrication process using conforming layers (Park et al., FIG. 8, column 6 lines 31-35) with an interconnect fabrication process using planar layers (Uzoh et al., FIG. 8c, column 6 lines 42-44 and 58-59). In addition, the Appellants note that Park et al. teaches away from a planarization step following the formation of the first conductive layer (column 6 lines 37-38) as taught by Uzoh et al. (column 4 lines 40-44). Moreover, the Appellants submit that one skilled in the art would not combine a process that teaches an anneal after the formation of the second conductive layer (Uzoh et al., column 7 lines 49-50) with a that teaches away from the use of an anneal s tep after the deposition of the second metal film (Park et al., column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Therefore, Claim 5 is patentable over the patents granted to Park et al. and Uzoh et al.

Claim 6

Claim 6 is dependent on Claim 5 and is therefore allowable for the same reasons that Claims 1 and 5 are allowable. Furthermore, Claim 6 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claims 1 and 5, are not taught nor suggested by the patents granted to Park et al . or Uzoh et al.; either alone or in combination. Namely, Claim 6 further specifies that the annealing step is performed within a temperature range of 100º C to 300º C for a time between 10 minutes to 60 minutes.

Uzoh et al. does not teach the advantageously claimed invention because Uzoh et al. teaches an anneal step that is used in a completely different process. Specifically, Uzoh et al. teaches away from the advantageously claimed invention b y teaching a process where the first conductive layer is modified (by planarization and annealing) before the formation of the second conductive layer (column 4 lines 2534 and 62-67, column 5 lines 1-35), but not the formation of a second layer of copper grains over a first layer of copper grains having the first initial grain size as is advantageously claimed. As stated in column 1 lines 35-36, annealing promotes grain growth. The planarization process also

modifies the grain size of the first conductive layer (column 5 lines 35-67, column 6 lines 1-28).

Park et al. does not teach the advantageously claimed anneal step because Park et al. only teaches the use of an anneal step after the deposition of the first metal film (column 2 lines 35-36 and 62-64, column 3 lines 29-33, column 4 lines 36-37, column 5 lines 49-51). Furthermore, the Appellants submit that Park et al. teaches away from the use of an anneal step after the deposition of the second metal film by teaching that the planarization step is performed "immediately" after the second metal film is deposited (column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Furthermore, the Appellants submit that one skilled in the art would not combine the teachings of an interconnect fabrication process using conforming layers (Park et al., FIG. 8, column 6 lines 31-35) with an interconnect fabrication process using planar layers (Uzoh et al., FIG. 8c, column 6 lines 42-44 and 58-59). In addition, the Appellants note that Park et al. teaches away from a planarization step following the formation of the first conductive layer (column 6 lines 37-38) as taught by Uzoh et al. (column 4 lines 40-44). Moreover, the Appellants submit that one skilled in the art would not combine a process that teaches an anneal after the formation of the second conductive layer (Uzoh et al., column 7 lines 49-50) with a that teaches away from the use of an anneal step after the deposition of the second metal film (Park et al., column 2 lines 38-39 and 66-67, column 3 lines 34-36).

Therefore, Claim 6 is patentable over the patents granted to Park et al. and Uzoh et al.

ADDITIONAL ARGUMENTS

Claim 2

Claim 2 is dependent on Claim 1 and is therefore allowable for the same reasons that Claim 1 is allowable. Furthermore, Claim 2 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claim 1, are not taught nor suggested by the patents granted to Park et al. or Uzoh et al.; either alone or in combination. Namely, Claim 2 further specifies the additional step of depositing at least one additional layer of copper grains of any initial grain size over the second layer of copper grains, the at least one additional layer of copper grains being deposited by an electroplating process. Moreover, the patentability of Claim 2 is noted on page 9 of the Office Action. Therefore, Claim 2 is patentable over the patents granted to Park et al. and Uzoh et al.

Claim 4

Claim 4 is dependent on Claim 2 and is therefore allowable for the same reasons that Claims 1 and 2 are allowable. Furthermore, Claim 4 is allowable on its own merits because it recites additional features of the invention that, in combination with the limitation of Claims 1 and 2, are not taught nor suggested by the patents granted to Park et al. or Uzoh et al.; either alone or in combination. Namely, Claim 4 further specifies that an initial grain size of the at least one additional layer of copper grains is larger than the

first initial grain size . Moreover, the patentability of Claim 4 is noted on page 9 of the Office Action. Therefore, Claim4 is patentable overthe patents granted to Park et al. and Uzoh et al.

CONCLUSION

For the reasons stated above, the Appellants respectfully contend that each claim is patentable. Therefore, the reversal of all rejections is courteously solicited.

Respectfully submitted,

/Rose Alyssa Keagy/

Rose Alyssa Keagy

Attorney for Appellants

Reg. No. 35,095

Texas Instruments Incorporated

PO BOX 655474, M/S 3999

Dallas, TX 75265

972/917-4167

FAX - 972/917-4409/4418

CLAIMS APPENDIX

1. A method of manufacturing copper interconnects on a semiconductor wafer comprising:

forming a layer of patterned dielectric material, said patterned dielectric material defining spaces for said copper interconnects;

depositing a copper seed layer over said layer of patterned dielectric material;

depositing a first layer of copper grains having a first initial grain size over said copper seed layer, said first layer of copper grains being deposited by an electroplating process; and

depositing a second layer of copper grains having a second initial grain size over said first layer of copper grains having said first initial grain size, said second layer of copper grains being deposited by an electroplating process.

2. The method of Claim 1 further comprising depositing at least one additional layer of copper grains of any initial grain size over said second layer of copper grains, said at least one additional layer of copper grains being deposited by an electroplating process.

3. The method of Claim 1 wherein said first initial grain size is smaller than said second initial grain size.

4. The method of Claim 2 wherein an initial grain size of said at least one additional layer of copper grains is larger than said first initial grain size.

5. The method of Claim 1 further comprising annealing said semiconductor wafer after said step of depositing a second layer of copper grains.

6. The method of Claim 5 wherein said annealing step is performed within a temperature range of 100º C to 300º C for a time between 10 minutes to 60 minutes.

7. A method of manufacturing copper interconnects on a semiconductor wafer comprising:

forming a layer of patterned dielectric material, said patterned dielectric material defining spaces for said copper interconnects;

depositing a copper seed layer over said layer of patterned dielectric material;

depositing a first layer of copper grains having a first initial grain size over said copper seed layer, said first layer of copper grains being deposited by an electroplating process; and

depositing at least one additional layer of copper grains of differing initial grain sizes over said first layer of copper grains having said first initial grain size, said at least one additional layer of copper grains being deposited by an electroplating process.

8. A method of manufacturing copper interconnects on a semiconductor wafer comprising:

forming a layer of pattern ed dielectric material, said patterned dielectric material defining spaces for said copper interconnects;

depositing a copper seed layer over said layer of patterned dielectric material;

depositing a first layer of copper grains having a first initial grai n size over said copper seed layer, said first layer of copper grains being deposited by an electroplating process;

depositing a second layer of copper grains having a second initial grain size over said first layer of copper grains having said first initi al grain size , said second layer of copper grains being deposited by an electroplating process and said second initial grain size being larger than said first initial grain size; and

annealing said semiconductor wafer.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None